Docket No.: J0658.0014
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Robert E. Ober et al.

Application No.: 10/712,473 Confirmation No.: 9335

Filed: November 12, 2003 Art Unit: 2183

For: INTERRUPT AND TRAP HANDLING IN AN EMBEDDED MULTI-THREAD PROCESSOR TO AVOID PRIORITY INVERSION AND MAINTAIN REAL-TIME OPERATION

Examiner: B. P. Johnson

REPLY BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Reply Brief is pursuant to 37 CFR § 41.41(a), and is responsive to the Examiner's Answer mailed on July 5, 2007, in the above identified U.S. Patent application. As required under § 41.41(a), this Reply Brief is filed within two months of the Examiner's Answer.

No fees are believed due for the filing of this Reply Brief. However, if any fee is due, the Patent Office is authorized to charge such fee to Deposit Account No. 50-2215.

As described in Appellants' Appeal Brief, each of the claims under final rejection is patentable over the references cited by the Examiner. Appellant maintains each argument presented in the Brief.

In the "(10) Response to Arguments" section part "A. Claim 1" of the Examiner's Answer, the Examiner asserts that the interrupt threshold value is not recited as being "fixed". Appellant

agrees. However, in claim 1 an "interrupt threshold value is specified," and the specified interrupt threshold value is compared with an interrupt priority value of a requested interrupt. Thus there is inherently claimed a common or global threshold value that is used for comparison with interrupt priority values of requested interrupts. In contrast, Hobbs compares the priorities of two different processor functions (i.e., code thread and interrupt). This is different from determining whether a priority value of an interrupt is higher than a specified threshold value, as claimed. In fact, Hobbs does even suggest a threshold value.

In the "(10) Response to Argument" section part "B. Claim 22", the portion of Hobbs to which the Examiner refers does not teach a common threshold interrupt value, as claimed. Hobbs in col. 2, lines 50-54, states the following:

> These more complex systems usually include registers which permit respective priorities to be assigned to various interrupts and also permit a priority to be assigned to the *program or code thread currently being executed by the processor*.

(Emphasis added.) The Examiner is misinterpreting this citation. The word "thread" is applicable to both to "program" and to "code." The citation does not teach a "program" or "code thread;" it teaches a "program thread" or a "code thread." Hobbs therefore does not teach assigning a priority to an entire program. Moreover, as asserted above, Hobbs does not each suggest a threshold value.

With reference to "(10) Response to Argument" section part "C. Claim 25" and part "D. Claim 29", Hobbs compares the priorities of two different processor functions (i.e., code thread and interrupt). Hobbs does not suggest generating or specifying an interrupt threshold value, as claimed, and thus certainly does not comparing an interrupt priority value with an interrupt threshold value.

The other specific arguments relating to the patentability of the claims set forth in the Appeal Brief are maintained.

For at least the reasons set forth above, and those identified in the Appeal Brief, Appellants respectfully submit that the claims are patentable over the applied references. Accordingly, reversal of the final rejection of all claims is respectfully requested.

Dated: July 24, 2007

Respectfully submitted,

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